Data Sheet | November 2001 | File Number 9046

Radiation Hardened CMOS Dual SPDT Analog Switch

The HS-303RH analog switch is a monolithic device fabricated using Radiation Hardened CMOS technology and the Intersil dielectric isolation process for latch-up free operation. Improved total dose hardness is obtained by layout (thin oxide tabs extending to a channel stop) and processing (hardened gate oxide). This switch offers low-resistance switching performance for analog voltages up to the supply rails. "ON" resistance is low and stays reasonably constant over the full range of operating voltage and current. "ON" resistance also stays reasonably constant when exposed to radiation, being typically 30Ω pre-rad and 35Ω post 100kRAD(Si). Break-before-make switching is controlled by 5V digital inputs.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the HS-303RH are contained in SMD 5962-95813. A "hot-link" is provided from our website for downloading

Ordering Information

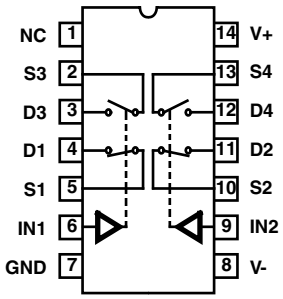
ORDERING NUMBER	PART NUMBER	TEMP. RANGE (^{o}C)
5962R9581301QCC	HS1-303RH-8	-55 to 125
5962R9581301QXC	HS9-303RH-8	-55 to 125
5962R9581301VCC	HS1-303RH-Q	-55 to 125
5962R9581301VXC	HS9-303RH-Q	-55 to 125
HS1-303RH/PROTO	HS1-303RH/PROTO	-55 to 125
HS9-303RH/PROTO	HS9-303RH/PROTO	-55 to 125

Features

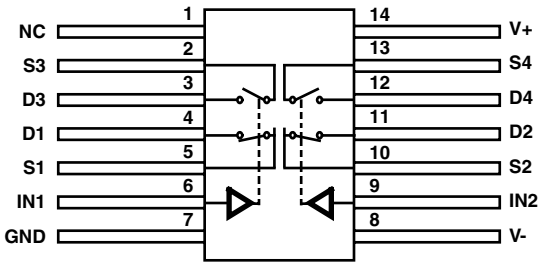
- QML, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose (γ) 1 x 10^5 RAD(Si)
- No Latch-Up, Dielectrically Isolated Device Islands
- Pin for Pin Compatible with Intersil HI-303 Series Analog Switches
- Analog Signal Range 15V
- Low Leakage . . . . . 100nA (Max, Post Rad)
- Low r_{ON} . . . . . 60Ω (Max, Post Rad)
- Low Operating Power . . . . . 100μA (Max, Post Rad)

Pinouts

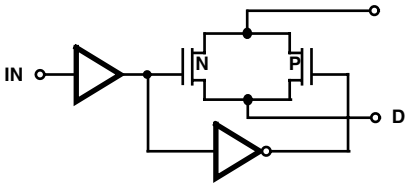
HS1-303RH (SBDIP), CDIP2-T14
TOP VIEW



HS9-303RH (FLATPACK) CDFP3-F14
TOP VIEW



Functional Diagram



SBDIP TRUTH TABLE

LOGIC	SW1AND SW2	SW3 AND SW4
0	OFF	ON
1	ON	OFF

Die Characteristics

DIE DIMENSIONS:

(2130μm x 1930μm x 279μm ±25.4μm)
84 x 76 x 11mils ±1mil

METALLIZATION:

Type: Al
Thickness: 12.5kÅ ±2kÅ

SUBSTRATE POTENTIAL:

Unbiased (DI)

BACKSIDE FINISH:

Gold

PASSIVATION:

Type: Silox (S_iO_2)
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm^2

TRANSISTOR COUNT:

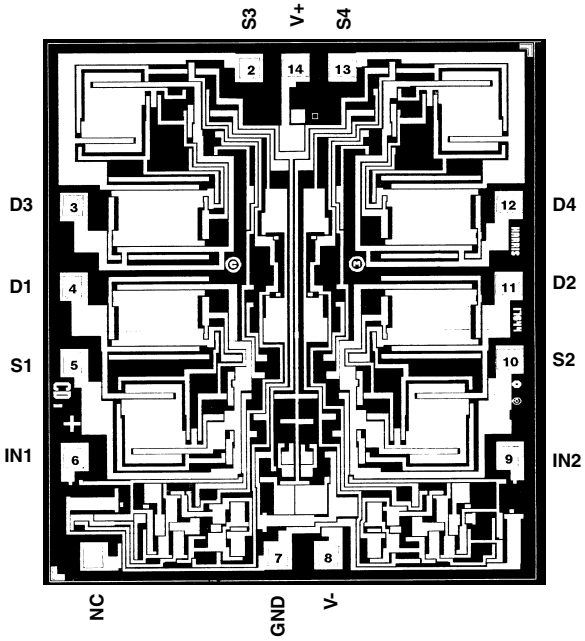
76

PROCESS:

Metal Gate CMOS, Dielectric Isolation

Metallization Mask Layout

HS-303RH-T



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Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality